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10/065,524	10/25/2002	Chau-Chad Tsai	JCLA8269	2141

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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,524	TSAI ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

3. Claims 2, 3, 6, 7, 10, and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 2, 6, and 10 recite the limitations that "the first control chip is a north-bridge chip" and "the second control chip is a south bridge chip". It is unclear from the claims and specification as to what the north-bridge and south-bridge chips are, as Claims 1, 5, and 9, from which Claims 2, 6, and 10 depend, respectively, make no mention of the control chips performing a bridging function. The nomenclature of north and south refers to whether a device is above (north) or below (south) of an intermediate bus, such as a PCI bus, on a block diagram. For the purposes of evaluating prior art, the Examiner will interpret a north bridge to be a bridge that interfaces a CPU local bus with an intermediate bus, and a south bridge to be a bridge that interfaces an intermediate bus with a peripheral bus.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,628,001 to Cepuran ("Cepuran").

6. In reference to Claim 1, Cepuran discloses a method of hot switching a data transfer rate on a bus, to dynamically switch the data transfer rate on the bus between a first control chip (See Figure 2 Number 106) and a second control chip (See Figure 2 Number 112), comprising the steps of: the first control chip and the second control chip receiving a transfer rate switching command (See Figure 2 Numbers 154 and 160); when either there is no data transaction processed or the data transaction process is finished, the first control chip issuing a bus release connect command (See Figure 1 Number 166; Figure 7 Numbers 706 and 718; and Column 5 Line 51 – Column 6 Line 13); the first control chip and the second control chip entering into the bus release connect state according to the bus release connect command (See Column 6 Lines 7-13); the first control chip issuing a bus re-connect command (See Figure 7 Number 712

and Column 5 Line 63 – Column 6 Line 6); and the first control chip and the second control chip re-connecting to the rated-changed bus according to the transfer rate switching command (See Figure 7 Number 712 and Column 5 Line 63 – Column 6 Line 6).

7. In reference to Claim 5, Cepuran discloses a method of hot switching a data transfer rate on a bus, comprising the steps of: receiving a transfer rate switching signal (See Figure 2 Numbers 154 and 160) before data transfer on the bus between a first control chip (See Figure 2 Number 106) and a second control chip (See Figure 2 Number 112) is interrupted; and after states of the first control chip and the second control chip are changed from a bus release state (See Column 6 Lines 7-13) into a re-connecting state (See Figure 7 Number 712 and Column 5 Line 63 – Column 6 Line 6), providing another data transfer rate to the bus according to the transfer rate switching signal (See Figure 7 Number 712 and Column 5 Line 63 – Column 6 Line 6).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 3, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran as applied to Claims 1 and 5 above, and further in view of US Patent Number 6,148,357 to Gulick et al. ("Gulick").

10. In reference to Claim 2, Cepuran teaches the limitations as applied to Claim 1 above. Cepuran does not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Gulick teaches a system having a north-bridge chip (See Figure 2 Number 201) and a south-bridge chip (See Figure 2 Number 211) connected by an interconnect (See Figure 2 Number 209).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Gulick with the interconnect between circuit elements having an adjustable clock frequency of Cepuran, resulting in the invention of Claim 2, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

11. In reference to Claim 3, Cepuran and Gulick teach the limitations as applied to Claim 2 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Gulick do not expressly teach that the data transfer rate is switched between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being

between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the invention of Claim 3, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious to one of ordinary skill in the art to modify Cepuran and Gulick to obtain the invention as specified in Claim 3.

12. In reference to Claim 6, Cepuran teaches the limitations as applied to Claim 5 above. Cepuran does not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Gulick teaches a system having a north-bridge chip (See Figure 2 Number 201) and a south-bridge chip (See Figure 2 Number 211) connected by an interconnect (See Figure 2 Number 209).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Gulick with the interconnect between

circuit elements having an adjustable clock frequency of Cepuran, resulting in the invention of Claim 6, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

13. In reference to Claim 7, Cepuran and Gulick teach the limitations as applied to Claim 6 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Gulick do not expressly teach that the data transfer rate is switched between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the invention of Claim 7, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious

to one of ordinary skill in the art to modify Cepuran and Gulick to obtain the invention as specified in Claim 3.

14. Claims 2, 3, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran as applied to Claims 1 and 5 above, and further in view of US Patent Application Publication Number 2002/0023190 to Peng ("Peng").

15. In reference to Claim 2, Cepuran teaches the limitations as applied to Claim 1 above. Cepuran does not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Peng teaches a system having a north-bridge chip (See Figure 1B Number 10') and a south-bridge chip (See Figure 1B Number 20') connected by an interconnect (See Figure 1B Number 20V).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peng with the interconnect between circuit elements having an adjustable clock frequency of Cepuran, resulting in the invention of Claim 2, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

16. In reference to Claim 3, Cepuran and Peng teach the limitations as applied to Claim 2 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Peng do not expressly teach that the data transfer rate is switched

between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the invention of Claim 3, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious to one of ordinary skill in the art to modify Cepuran and Peng to obtain the invention as specified in Claim 3.

17. In reference to Claim 6, Cepuran teaches the limitations as applied to Claim 5 above. Cepuran does not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Peng teaches a system having a north-bridge chip (See Figure 1B Number 10') and a south-bridge chip (See Figure 1B Number 20') connected by an interconnect (See Figure 1B Number 20V).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peng with the interconnect between circuit elements having an adjustable clock frequency of Cepuran, resulting in the invention of Claim 6, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

18. In reference to Claim 7, Cepuran and Peng teach the limitations as applied to Claim 6 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Peng do not expressly teach that the data transfer rate is switched between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the invention of Claim 7, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio

taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious to one of ordinary skill in the art to modify Cepuran and Peng to obtain the invention as specified in Claim 3.

19. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran as applied to Claims 1 and 5 above, and further in view of US Patent Number 6,057,729 to Nomura ("Nomura").

20. In reference to Claim 4, Cepuran teaches the limitations as applied to Claim 1 above. Cepuran does not teach that the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command. Cepuran teaches that the transfer rate switching command is a clock signal (See Figure 2 Numbers 154 and 160). Nomura teaches temporarily storing a received clock signal in a register (See Figure 6 and Column 6 Line 65 – Column 7 Line 19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Cepuran with the clock registers of Nomura, resulting in the invention of Claim 4, in order to control the parasitic elements in accordance with the clock signal (See Column 3 Lines 5-46 and Column 7 Lines 13-16 of Nomura).

21. In reference to Claim 8, Cepuran teaches the limitations as applied to Claim 5 above. Cepuran does not teach that the first control chip and the second control chip both have a transfer rate register for temporarily storing the transfer rate switching command. Cepuran teaches that the transfer rate switching command is a clock signal (See Figure 2 Numbers 154 and 160). Nomura teaches temporarily storing a received clock signal in a register (See Figure 6 and Column 6 Line 65 – Column 7 Line 19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Cepuran with the clock registers of Nomura, resulting in the invention of Claim 8, in order to control the parasitic elements in accordance with the clock signal (See Column 3 Lines 5-46 and Column 7 Lines 13-16 of Nomura).

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran and Nomura.

23. In reference to Claim 9, Cepuran discloses a method of hot switching a data transfer rate on a bus, to dynamically switch the data transfer rate on the bus between a first control chip (See Figure 2 Number 106) and a second control chip (See Figure 2 Number 112), comprising the steps of: the first control chip and the second control chip receiving a transfer rate switching command (See Figure 2 Numbers 154 and 160); when either there is no data transaction processed or the data transaction process is finished, issuing a bus release connect command (See Figure 1 Number 166; Figure 7

Numbers 706 and 718; and Column 5 Line 51 – Column 6 Line 13) to have the first control chip and the second control chip enter into a bus release connect state (See Column 6 Lines 7-13); and when either the first control chip or the second control chip issues a bus re-connect command (See Figure 7 Number 712 and Column 5 Line 63 – Column 6 Line 6), the first control chip and the second control chip switching to one of the data transfer rates on the bus according to the transfer rate switching command (See Figure 7 Number 712 and Column 5 Line 63 – Column 6 Line 6). Cepuran does not teach temporarily storing the transfer rate switching command into transfer rate registers of the first control chip and the second control chip. Cepuran teaches that the transfer rate switching command is a clock signal (See Figure 2 Numbers 154 and 160). Nomura teaches temporarily storing a received clock signal in a register (See Figure 6 and Column 6 Line 65 – Column 7 Line 19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Cepuran with the clock registers of Nomura, resulting in the invention of Claim 9, in order to control the parasitic elements in accordance with the clock signal (See Column 3 Lines 5-46 and Column 7 Lines 13-16 of Nomura).

24. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran and Nomura as applied to Claim 9 above, and further in view of Gulick.

25. In reference to Claim 10, Cepuran and Nomura teaches the limitations as applied to Claim 1 above. Cepuran and Nomura do not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Gulick teaches a system having a north-bridge chip (See Figure 2 Number 201) and a south-bridge chip (See Figure 2 Number 211).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Gulick with the interconnect between circuit elements having an adjustable clock frequency of Cepuran and Nomura, resulting in the invention of Claim 10, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

26. In reference to Claim 11, Cepuran and Gulick teach the limitations as applied to Claim 10 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Gulick do not expressly teach that the data transfer rate is switched between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the

invention of Claim 3, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious to one of ordinary skill in the art to modify Cepuran and Nomura and to obtain the invention as specified in Claim 3.

27. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepuran and Nomura as applied to Claim 9 above, and further in view of Peng.

28. In reference to Claim 10, Cepuran and Nomura teaches the limitations as applied to Claim 1 above. Cepuran and Nomura do not teach that the first control chip is a north-bridge chip and the second control chip is a south-bridge chip. Peng teaches a system having a north-bridge chip (See Figure 1B Number 10') and a south-bridge chip (See Figure 1B Number 20') connected by an interconnect (See Figure 1B Number 20V).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peng with the interconnect between circuit elements having an adjustable clock frequency of Cepuran and Nomura, resulting

in the invention of Claim 10, in order to reduce the power consumed by the interconnect (See Column 5 Lines 17-27 of Cepuran).

29. In reference to Claim 11, Cepuran and Peng teach the limitations as applied to Claim 10 above. Cepuran further discloses that the high-frequency clock signal is sixteen times that of the low-frequency clock signal (See Column 5 Lines 46-56). Cepuran and Peng do not expressly teach that the data transfer rate is switched between four times the north-bridge chip frequency and eight times the north-bridge chip frequency. The portion of the specification describing the switching as being between four times the north-bridge chip frequency and eight times the north-bridge chip frequency presents it as an exemplary embodiment with no further details.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to switch the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency, resulting in the invention of Claim 3, because Applicant has not disclosed that switching the data transfer rate between four times the north-bridge chip frequency and eight times the north-bridge chip frequency provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with either the switching ratio taught by Cepuran or the switching ratio taught by Applicant because both perform the same function of reducing power consumption. Therefore, it would have been obvious

to one of ordinary skill in the art to modify Cepuran, Nomura, and Peng to obtain the invention as specified in Claim 3.

Duty to Disclose

30. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56. Applicant is advised to submit any information material to patentability in accordance with 37 CFR 1.97 and 1.98.

Response to Arguments

31. Applicant's arguments with respect to Claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 6,079,022 to Young; US Patent Number 5,628,019 to O'Brien; US Patent Number 5,630,145 to Chen; US Patent Number

5,678,065 to Lee et al.; US Patent Number 5,491,814 to Yee et al; US Patent Number 5,625,807 to Lee et al.; US Patent Number 6,504,854 to Hofmann et al.; "Motherboards Page 2" webpage by Gen-X-PC; and "VIA KT400" webpage by VIA Technologies, Inc.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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